Direct Modulation/Fast Waveform Generating 13 GHz Fractional-N Frequency Synthesizer

Preliminary Technical Data

ADF4159

FEATURES

RF bandwidth to 13 GHz
High and low speed FMCW Ramps Generation
25-bit fixed modulus allows sub-hertz frequency resolution
PFD Frequencies up to 110MHz
Frequency and Phase modulation capability
Sawtooth and triangular waveforms generation
Parabolic ramp
Ramp superimposed with FSK
Ramp with 2 different sweep rates
Ramp Delay
Ramp Frequency Readback
Ramp Interruption
2.7 V to 3.3 V analog power supply
1.8 V digital power supply
Programmable charge pump currents
3-wire serial interface
Digital lock detect
Power-down mode
Cycle Slip Reduction for faster lock times
Switched Bandwidth Fast Lock Mode

APPLICATIONS

FMCW radar
Communications test equipment

GENERAL DESCRIPTION

The ADF4159 is a 13 GHz, fractional-N frequency synthesizer with modulation and both fast and slow waveform generation capability. It contains a 25-bit fixed modulus, allowing subhertz resolution at 13 GHz. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a sigma-delta (Σ-Δ) based fractional interpolator to allow programmable fractional-N division. The INT and FRAC registers define an overall N-divider as $N = INT + (FRAC/2^{25})$.

The ADF4159 can be used to implement frequency shift keying (FSK) and phase shift keying (PSK) modulation. There are also a number of frequency sweep modes available, which generate various waveforms in the frequency domain, for example, sawtooth and triangular waveforms. The ADF4159 features cycle slip reduction circuitry, which leads to faster lock times, without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with an analog power supply in the range from 2.7 V to 3.3 V and digital power supply in the range from 1.6 V to 2 V. It can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

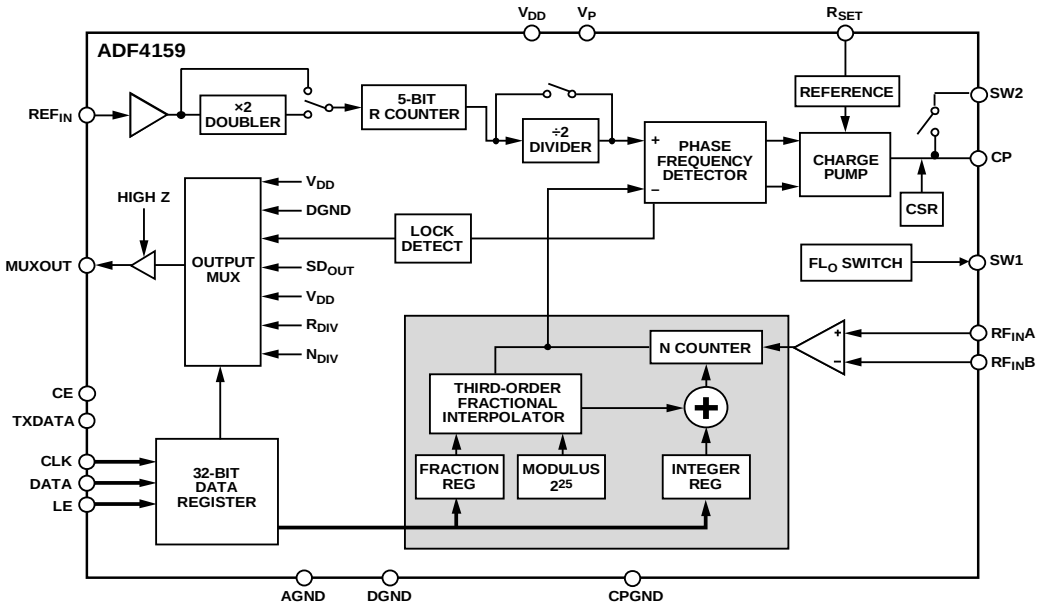

Figure 1.

Rev. PrC

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SPECIFICATIONS

AV_{DD} = 2.7 V to 3.3 V, DV_{DD} = SDV_{DD} = 1.8V; V_P = AV_{DD}, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 1.

	C Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
RF CHARACTERISTICS					
RF Input Frequency (RF_{IN})	0.5		13	GHz	−10 dBm min to 0 dBm max; for lower frequencies, ensure slew rate (SR) > 400 V/µs
REFERENCE CHARACTERISTICS					
REF_{IN} Input Frequency	10		260	MHz	For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 25 V/µs
			TBD	MHz	If an internal reference doubler is enabled
REF_{IN} Input Sensitivity		TBD		V p-p	Biased at 1.8/2[2]
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[3]			110	MHz	
CHARGE PUMP					
I_{CP} Sink/Source					Programmable
High Value		5		mA	With R_{SET} = 5.1 kΩ
Low Value		312.5		µA	
Absolute Accuracy		2.5		%	With R_{SET} = 5.1 kΩ
R_{SET} Range	2.7		10	kΩ	
I_{CP} Three-State Leakage Current		1		nA	Sink and source current
Matching		2		%	0.5 V < V_{CP} < V_P – 0.5 V
I_{CP} vs. V_{CP}		2		%	0.5 V < V_{CP} < V_P – 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
V_{INH}, Input High Voltage	1.4			V	
V_{INL}, Input Low Voltage			0.6	V	
I_{INH}/I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen; 1 kΩ pull-up to 1.8 V
V_{OH}, Output High Voltage	V_{DD} – 0.4			V	CMOS output chosen
I_{OH}, Output High Current			100	µA	
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}	1.6	1.8	2	V	
SDV_{DD}	1.6	1.8	2	V	
V_P	2.7		3.3	V	
I_{DD}		33	42	mA	

Parameter	C Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[4]		TBD		dBc/Hz	PLL loop BW = 500 kHz
Normalized 1/f Noise (PN_{1_f})[5]		TBD			Measured at 10 kHz offset, normalized to 1 GHz
Phase Noise Performance[6]					@ VCO output
12000 MHz Output[7]		TBD		dBc/Hz	@ 50 kHz offset, 100 MHz PFD frequency

[1] Operating temperature for C version: −40°C to +125°C.
[2] AC-coupling ensures 1.8/2 bias.
[3] Guaranteed by design. Sample tested to ensure compliance.
[4] This figure can be used to calculate phase noise for any application. Use the formula TBD + 10 log(f_{PFD}) + 20 logN to calculate in-band phase noise performance as seen at the VCO output.
[5] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, F_{RF}, and at an offset frequency, f, is given by PN = P_{1_f} + 10 log(10 kHz/f) + 20 log(F_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[6] The phase noise is measured with the EVAL-ADF4159EB1Z and the Agilent E5052A phase noise system.
[7] fREFIN = 100 MHz; fPFD = 100 MHz; offset frequency = 50 kHz; RFOUT = 12000 MHz; N = 120; loop bandwidth = 200 kHz.

TIMING SPECIFICATIONS

AV_{DD} = 2.7 V to 3.3 V; DV_{DD} = SDV_{DD} = 1.8V; V_P = AV_{DD}; AGND = DGND = SDGND = 0V; T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 2. Write Timing

Parameter	Limit at T_{MIN} to T_{MAX} (C Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Write Timing Diagram

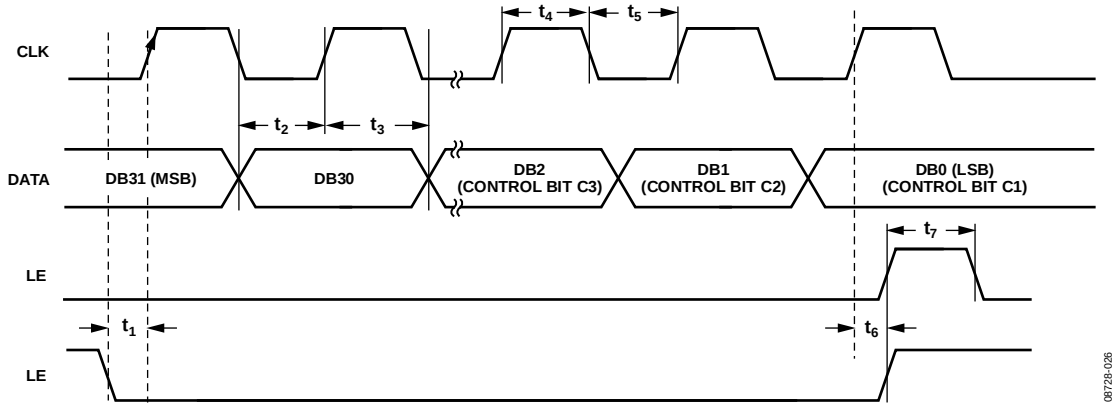


Figure 2. Write Timing Diagram

Table 3. Read Timing

Parameter	Limit at T_{MIN} to T_{MAX} (C Version)	Unit	Test Conditions/Comments
t_1	20	ns min	TX_{DATA} setup time
t_2	10	ns min	DATA (on MUXOUT) to CLK setup time
t_3	10	ns min	DATA (on MUXOUT) to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time

Read Timing Diagram

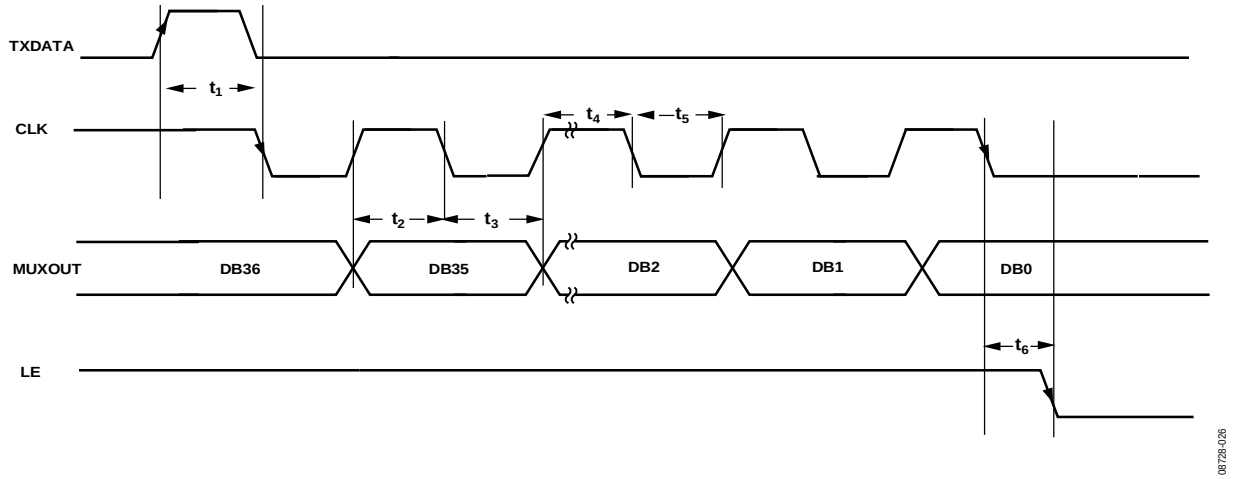


Figure 3. Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = SDGND = 0 V,
V_{DD} = AV_{DD} , DV_{DD} = SDV_{DD}, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +4 V
DV_{DD} to GND	−0.3 V to +2.4 V
V_P to GND	−0.3 V to +4 V
V_P to AV_{DD}	−0.3 V to +0.6 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (C Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

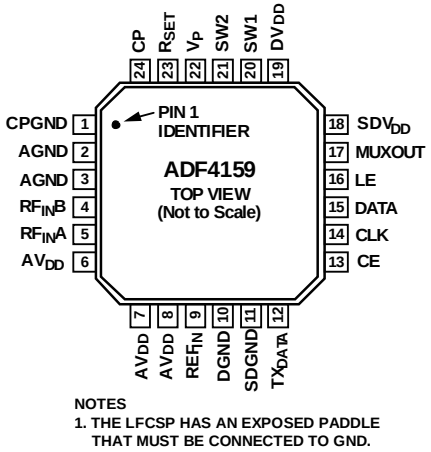


Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler. Decouple this point to the ground plane with a small bypass capacitor, typically 100 pF.
5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
6, 7, 8	AV_{DD}	Positive Power Supply for the RF Section. Place decoupling capacitors to the ground plane as close as possible to this pin.
9	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. It can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
10	DGND	Digital Ground.
11	SDGND	Digital Σ-Δ Modulator Ground. Ground return path for the Σ-Δ modulator.
12	TX_{DATA}	Tx Data Pin. Provide data to be transmitted in FSK or PSK mode on this pin.
13	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode.
14	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
15	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input.
16	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the eight latches, with the latch being selected using the control bits.
17	MUXOUT	Multiplexer Output. This pin allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
18	SDV_{DD}	Power Supply Pin for the Digital Σ-Δ Modulator. This pin should be 1.8V. Place decoupling capacitors to the ground plane as close as possible to this pin.
19	DV_{DD}	Positive Power Supply for the Digital Section. Place decoupling capacitors to the digital ground plane as close as possible to this pin. DV_{DD} must be 1.8V.
20 , 21	SW1, SW2	Switches for Fast Lock.
22	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. The max value of V_P is 3.3V.
23	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = \frac{25.5}{R_{SET}}$ where: I_{CPmax} = 5 mA. R_{SET} = 5.1 kΩ.
24	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
25	EPAD	Exposed Paddle. The LFCSP has an exposed paddle that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

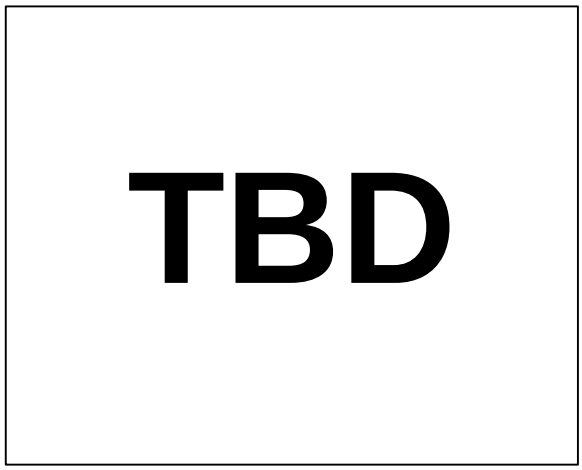


Figure 5.

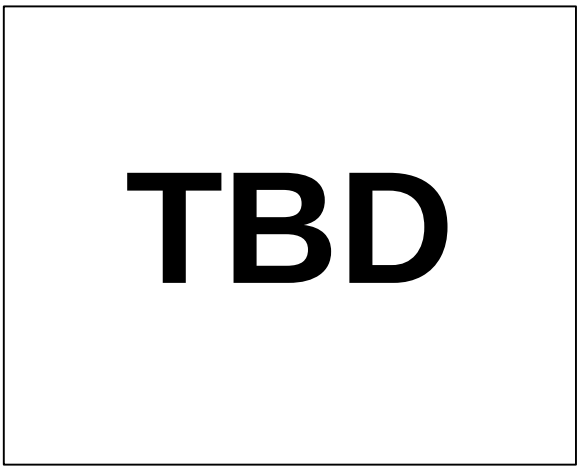


Figure 8

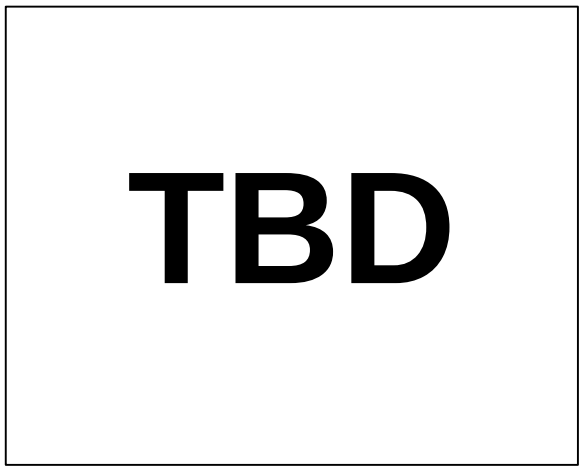


Figure 6

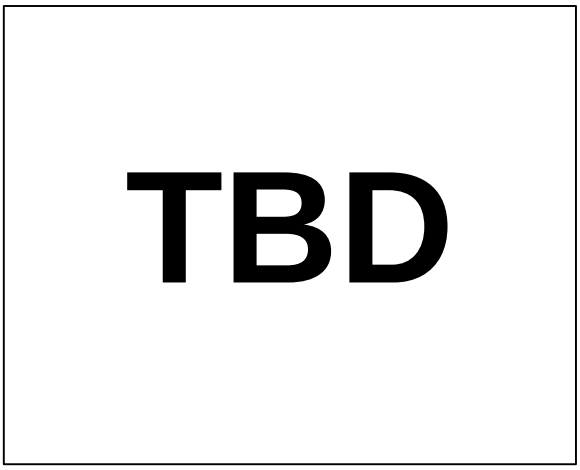


Figure 9.

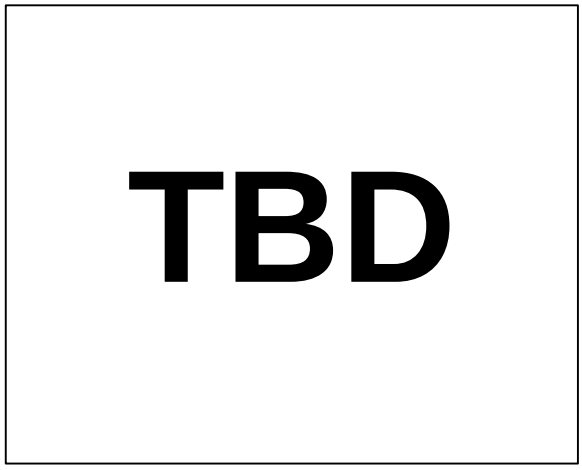


Figure 7.

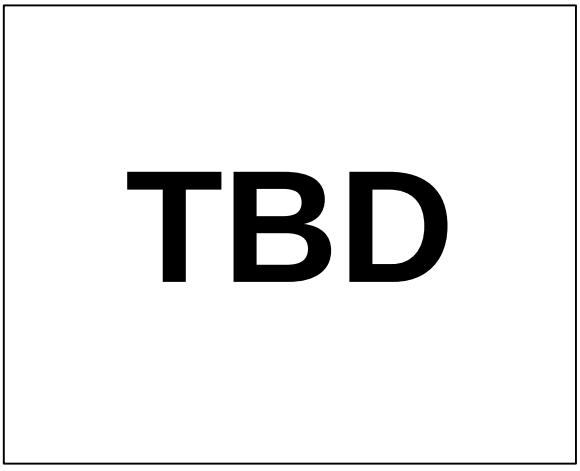


Figure 10

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 11. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

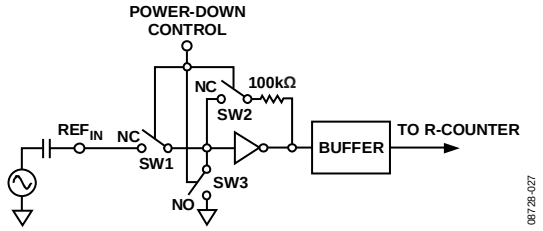


Figure 11. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 12. It is followed by a 2-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

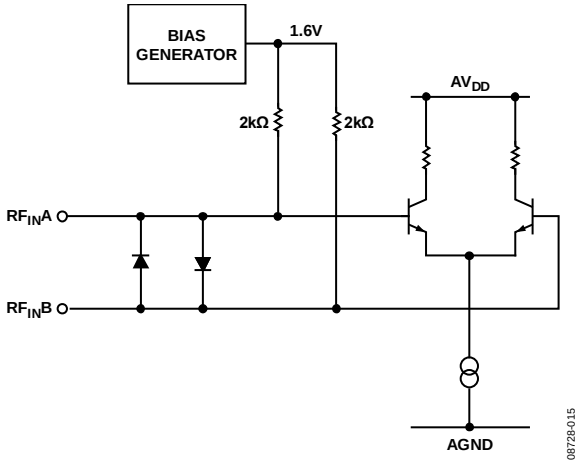


Figure 12. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

25-BIT FIXED MODULUS

The ADF4159 has a 25-bit fixed modulus. This allows output frequencies to be spaced with a resolution of

$$f_{RES} = f_{PFD}/2^{25} \quad (1)$$

where f_{PFD} is the frequency of the phase frequency detector (PFD). For example, with a PFD frequency of 10 MHz, frequency steps of 0.298 Hz are possible.

INT, FRAC, AND R RELATIONSHIP

The INT and FRAC values, in conjunction with the R-counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (2)$$

where:

RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

INT is the preset divide ratio of binary 12-bit counter (23 to 4095).

FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (3)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit (0 or 1).

T is the REF_{IN} divide-by-2 bit (0 or 1).

R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

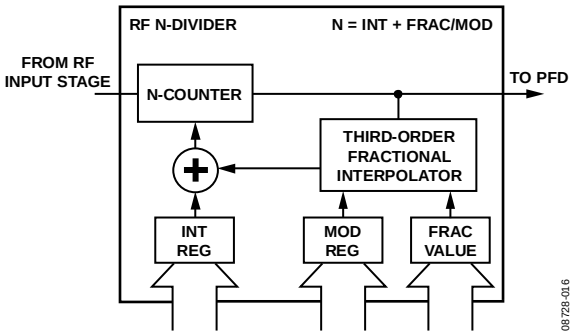


Figure 13. RF N-Divider

R-COUNTER

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R-counter and N-counter and produces an output proportional to the phase and frequency difference between them. Figure 14 shows a simplified schematic of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

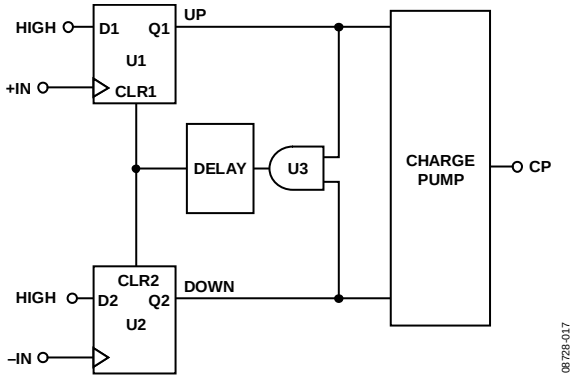


Figure 14. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4159 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M4, M3, M2, and M1 bits (see Figure 18). Figure 15 shows the MUXOUT section in block diagram form.

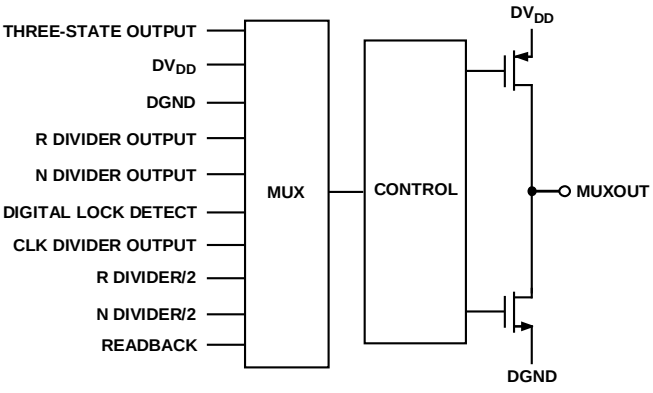


Figure 15. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4159 digital section includes a 5-bit RF R-counter, a 12-bit RF N-counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of eight latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These are the three LSBs—DB2, DB1, and DB0—as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 16 and Figure 17 show a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 18 through Figure 25 show how to set up the program modes in the ADF4159.

Several settings in the ADF4159 are double buffered. These include the LSB fractional value, R-counter value, reference doubler, current setting, and RDIV2. This means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, updating the fractional value can involve a write to the 13 LSB bits in R1 and the 12 MSB bits in R0. R1 should be written to first, followed by the write to R0. The frequency change begins after the write to R0. Double buffering ensures that the bits written to in R1 do not take effect until after the write to R0.

Table 6. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

REGISTER MAPS

FRAC/INT REGISTER (R0)

RAMP ON	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

LSB FRAC REGISTER (R1)

RESERVED			PHASE ADJ	13-BIT LSB FRACTIONAL VALUE (FRAC) (DBB)													12-BIT PHASE WORD (DBB)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	P1	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(0)	C1(1)

R DIVIDER REGISTER (R2)

RESERVED			CSR EN	DBB CURRENT SETTING				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	DBB 5-BIT R COUNTER					12-BIT MOD DIVIDER (DBB)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	C1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED														RESERVED	LOL EN	N SEL	SD RESET	RESERVED		RAMP MODE		PSK ENABLE	FSK ENABLE	LDP	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	L1	NS1	U12	0	0	RM2	RM1	PE1	FE1	U11	U10	U9	U8	U7	C3(0)	C2(1)	C1(1)

NOTES
1. DBB = DOUBLE BUFFERED BIT(S).

Figure 16. Register Summary 1

TEST REGISTER (R4)

LE SEL	RESERVED	READ BACK TO MUXOUT	CLK DIV MODE	12-BIT CLOCK DIVIDER VALUE	CLK DIV SEL	RESERVED	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LS1	0	0	0	0	0	0	0	0	R2	R1	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	CS1	0	0	0	C3(1)	C2(0)	C1(0)

DEV REGISTER (R5)

RESERVED	TX RAMP CLK	PAR RAMP	INTERRUPT	FSK RAMP EN	RAMP 2 EN	DEV SEL	4-BIT DEV OFFSET WORD	16-BIT DEVIATION WORD	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	TR1	PR1	I2	I1	FRE1	R2E1	DS1	DO4	DO3	DO2	DO1	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(0)

STEP REGISTER (R6)

RESERVED	STEP SEL	20-BIT STEP WORD	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	SSE1	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	C3(0)	C2(0)	C1(0)

DELAY REGISTER (R7)

RESERVED	TRI DELAY	SING FULL TRI	TX RB EN	FAST RAMP	RAMP DEL FL	RAMP DEL	DEL CLK SEL	DEL START EN	12-BIT DELAY START DIVIDER	CONTROL BITS

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	TD1	ST1	TR1	FR1	RDF1	RD1	DC1	DSE1	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	C3(0)	C2(0)	C1(1)

Figure 17. Register Summary 2

FRAC/INT REGISTER (R0) MAP

With Register R0 DB[2:0] set to [0, 0, 0], the on-chip FRAC/INT register is programmed as shown in Figure 18.

Ramp On

Setting DB31 to 1 enables the ramp, setting DB31 to 0 disables the ramp.

MUXOUT Control

The on-chip multiplexer is controlled by DB[30:27] on the ADF4159. See Figure 18 for the truth table.

12-Bit Integer Value (INT)

These 12 bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 2. See the INT, FRAC, and R Relationship section on Page 9 for more information.

12-Bit MSB Fractional Value (FRAC)

These 12 bits, along with Bits DB[27:15] in the LSB FRAC register (Register R1), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits DB[27:15] in the LSB FRAC register (Register R1) are the least significant bits (LSB). See the RF Synthesizer: A Worked Example section on Page 23 for more information.

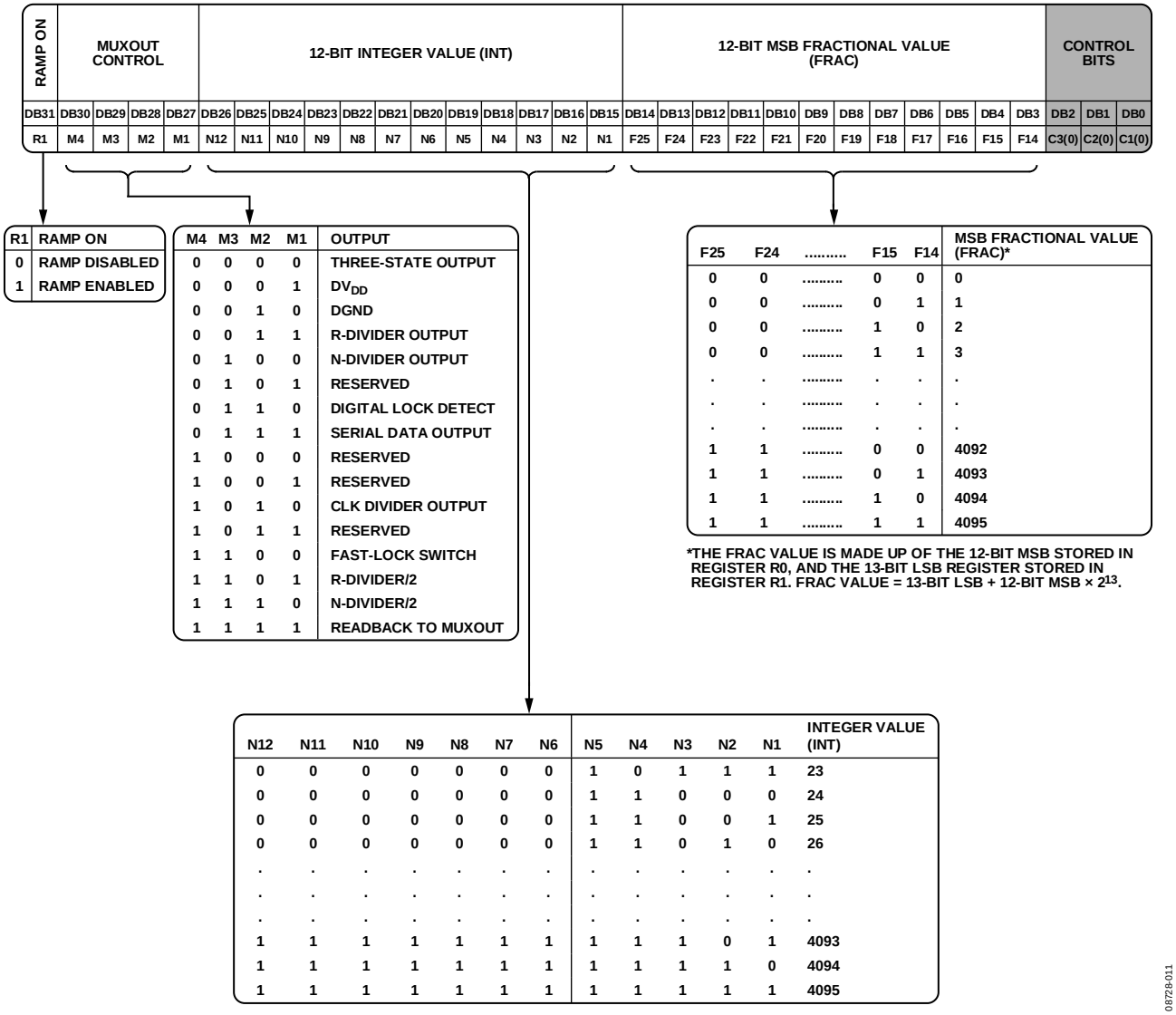


Figure 18. FRAC/INT Register (R0) Map

LSB FRAC REGISTER (R1) MAP

With Register R1 DB[2:0] set to [0, 0, 1], the on-chip LSB FRAC register is programmed as shown in Figure 19.

Phase Adj

This bit enables /disables phase adjustment. Phase of the generated signal is adjusted by the value programmed by bits DB[14:3] in Register R1 (12-bit Phase Value).

13-Bit LSB FRAC Value

These 13 bits, along with Bits DB[14:3] in the FRAC/INT register (Register R0), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 13 bits are the least significant bits (LSB) of the 25-bit FRAC value, and Bits DB[14:3] in the INT/FRAC register are the most significant bits (MSB). See the RF Synthesizer: A Worked Example section on Page 23 for more information.

12-Bit Phase Value

These twelve bits control what is loaded as the PHASE word. The word is used to program the RF output phase from 0° to 360 o with a resolution of 360o/2^{12}. The phase shift equals to $PhaseValue \cdot 360^0 / 2^{12}$. If the PHASE ADJUSTMENT is not being used, it is recommended that the PHASE word be set to 0.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

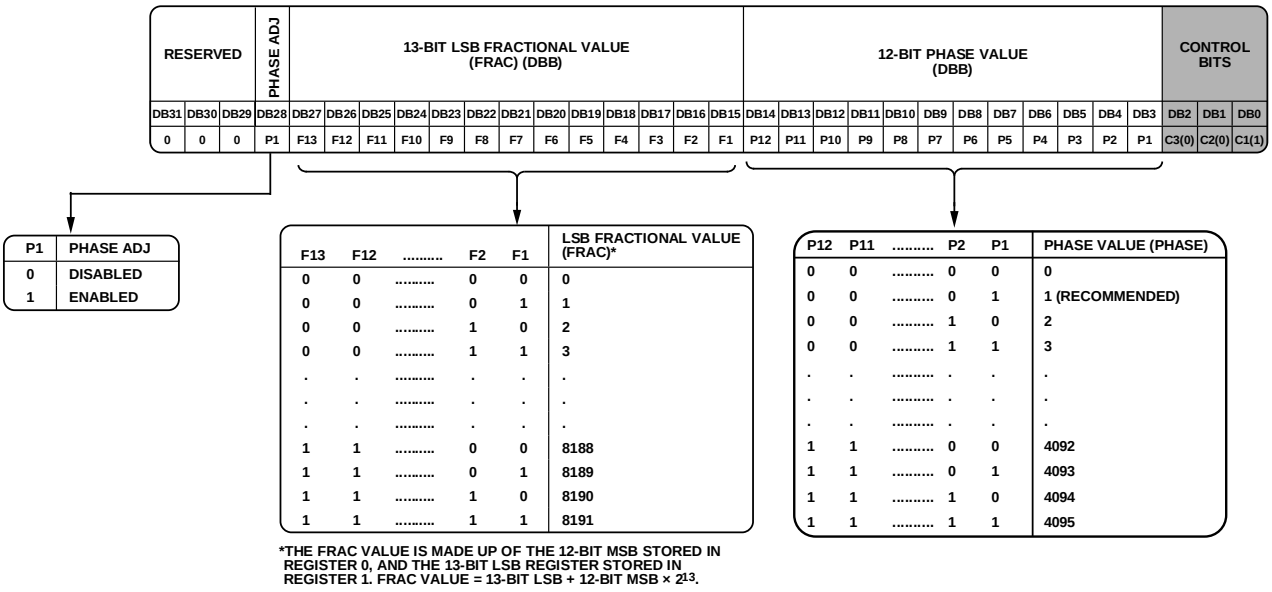


Figure 19. LSB FRAC Register (R1) Map

R-DIVIDER REGISTER (R2) MAP

With Register R2 DB[2:0] set to [0, 1, 0], the on-chip R-divider register is programmed as shown in Figure 20.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

CSR Enable

Setting this bit to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the PFD must have a 50% duty cycle in order for cycle slip reduction to work. In addition, the charge pump current setting must be set to a minimum. See the Cycle Slip Reduction for Faster Lock Times section on Page 23 for more information.

Also note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is set to negative.

Charge Pump Current Setting

DB[27:24] set the charge pump current setting (see Figure 20). Set these bits to the charge pump current that the loop filter is designed with.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4159 above 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value.

With P = 4/5, N_{MIN} = 23.

With P = 8/9, N_{MIN} = 75.

RDIV2

Setting DB21 to 1 inserts a divide-by-2 toggle flip-flop between the R-counter and the PFD. This can be used to provide a 50% duty cycle signal at the PFD for use with cycle slip reduction.

Reference Doubler

Setting DB20 to 0 feeds the REF_{IN} signal directly to the 5-bit RF R-counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding the signal into the 5-bit R-counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising edge and falling edge of REF_{IN} become active edges at the PFD input.

The maximum allowed REF_{IN} frequency when the doubler is enabled is 30 MHz.

5-Bit R-Counter

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 32 are allowed.

12-Bit MOD Divider

Bits DB[14:3] are used to program the MOD divider, which determines the duration of the time step in ramp mode.

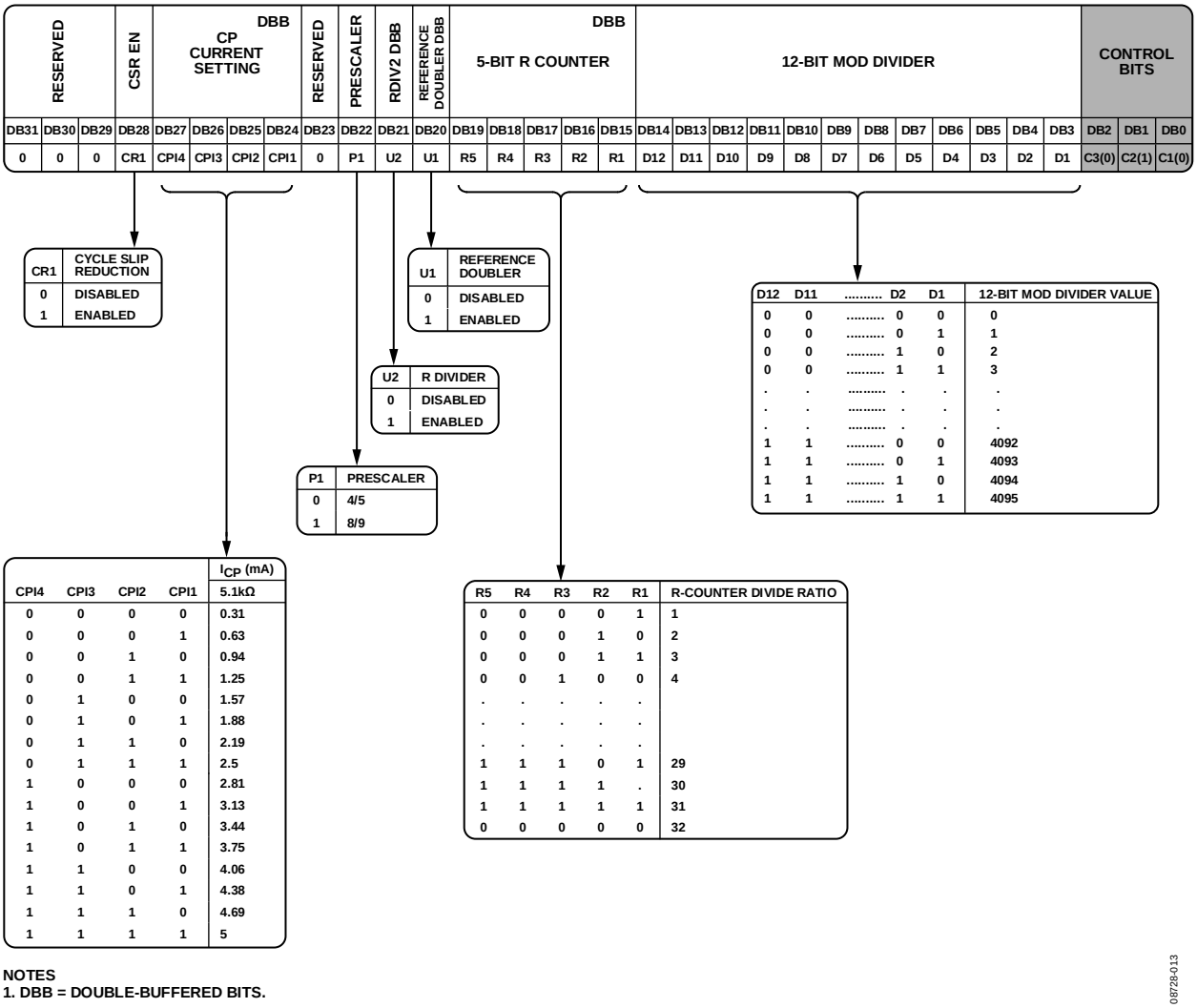


Figure 20. R-Divider Register (R2) Map

FUNCTION REGISTER (R3) MAP

With Register R3 DB[2:0] set to [0, 1, 1], the on-chip function register is programmed as shown in Figure 21.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Loss of Lock (LOL)

This bit enables/disables loss of lock indication. This setting indicates loss of lock even in the case of removing the reference which is a big advantage over the standard implementation of lock detect.

N SEL

This setting is used to circumvent the issue of pipeline delay between an update of the integer and fractional values in the N-counter. Typically, the INT value is loaded first, followed by the FRAC value. This can cause the N-counter value to be at an incorrect value for a brief period of time equal to the pipeline delay (about four PFD cycles). This has no effect if the INT value has not been updated. However, if the INT value has been changed, this can cause the PLL to overshoot in frequency while it tries to lock to the temporarily incorrect N value. After the correct fractional value is loaded, the PLL quickly locks to the correct frequency. Introducing an additional delay to the loading of the INT value using the N SEL bit causes the INT and FRAC values to be loaded at the same time, preventing frequency overshoot. The delay is turned on by setting Bit DB15 to 1.

SD Reset

For most applications, DB14 should be set to 0. When DB14 is set to 0, the Σ-Δ modulator is reset on each write to Register R0. If it is not required that the Σ-Δ modulator be reset on each Register R0 write, set this bit to 1.

Ramp Mode

DB[11:10] determine the type of generated waveform.

PSK Enable

When DB9 is set to 1, PSK modulation is enabled. When set to 0, PSK modulation is disabled.

FSK Enable

When DB8 is set to 1, FSK modulation is enabled. When set to 0, FSK modulation is disabled.

Lock Detect Precision (LDP)

When DB7 is programmed to 0, 24 consecutive PFD cycles of 15 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector (PD) Polarity

DB6 sets the phase detector polarity. When the VCO characteristics are positive, set this bit to 1. When the VCO characteristics are negative, set this bit to 0.

Power-Down

DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock-detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

Charge Pump Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

Counter Reset

DB3 is the RF counter reset bit. When this bit is set to 1, the RF synthesizer counters are held in reset. For normal operation, set this bit to 0.

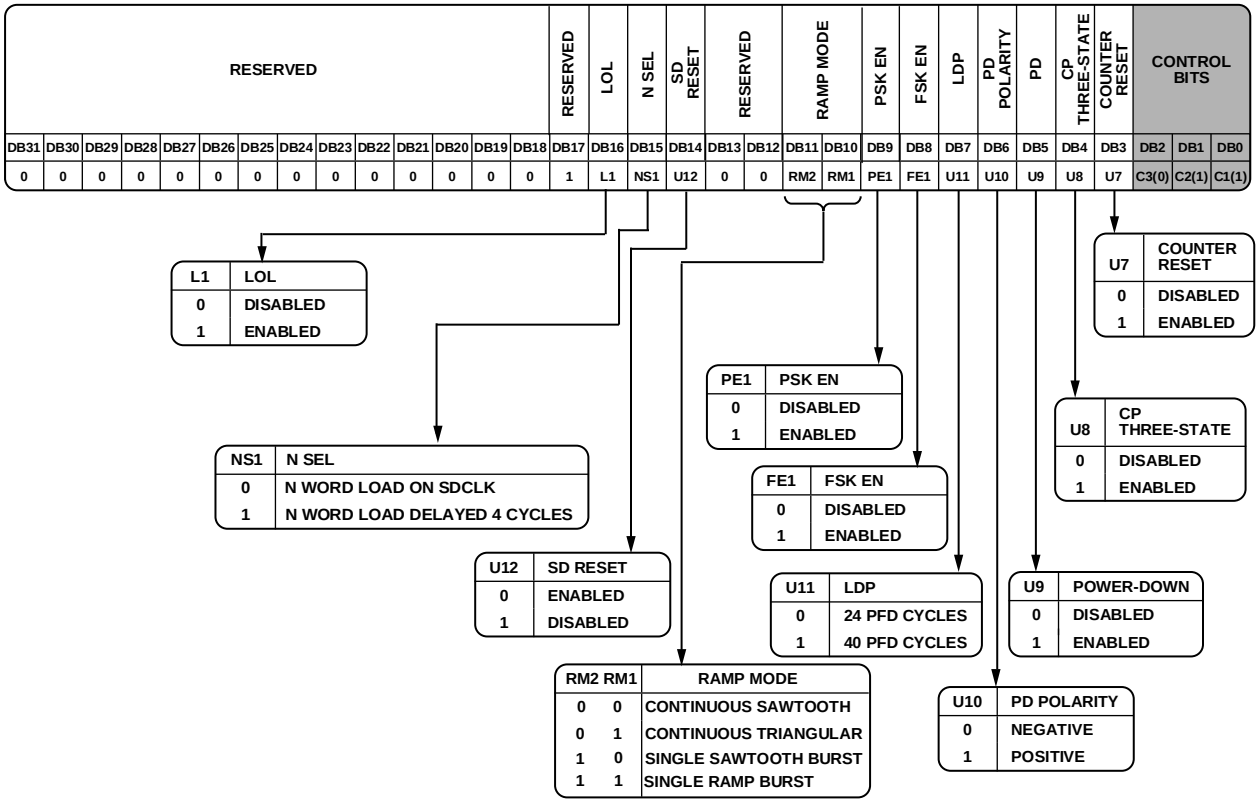


Figure 21. Function Register (R3) Map

TEST REGISTER (R4) MAP

With Register R4 DB[2:0] set to [1, 0, 0], the on-chip test register (R4) is programmed as shown in Figure 22.

LE SEL

In some applications, it is necessary to synchronize LE with the reference signal. To do this, DB31 should be set to 1. Synchronization is done internally on the part.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Readback to MUXOUT

DB[22:21] enable or disable the readback to MUXOUT function. This function allows reading back the synthesizer's frequency at the moment of interrupt.

CLK DIV Mode

Depending on the settings of DB[20:19], the 12-bit clock divider may be a counter for the switched R fast-lock ramp (CLK2), or it may be turned off.

12-Bit Clock Divider Value

DB[18:7] program the clock divider, which is used as a timer for ramp - CLK_2, while operating in ramp mode. See Waveform Deviations and Timing section on Page 25 for more details.The timer also determines how long the loop remains in wideband mode while the switched R fast-lock technique is used. See Fast-Lock Timer and Register Sequences on Page 30 for more details.

CLK DIV Sel

DB[6] selects which clock divider is loaded with 12-BIT CLOCK DIVIDER VALUE. It can be either clock divider one or clock divider two. These setting is used in the Fast Ramp Mode for programming the up and down ramp time step. Please see the Fast Ramp Mode section on Page 28 for more details.

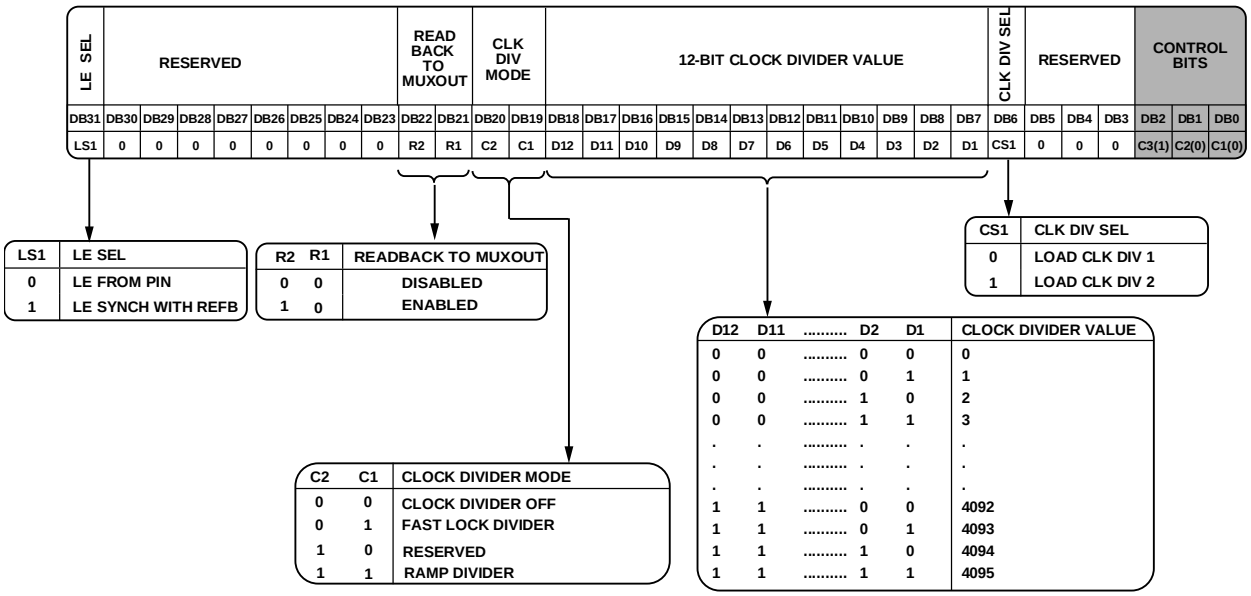


Figure 22. Test Register (R4) Map

DEVIATION REGISTER (R5) MAP

With Register R5 DB[2:0] set to [1, 0, 1], the on-chip deviation register is programmed as shown in Figure 23.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Tx Ramp CLK

Setting DB29 to 0 uses the clock divider clock for clocking the ramp. Setting DB29 to 1 uses the Tx data clock for clocking the ramp.

PAR Ramp

Setting DB28 to 1 enables the parabolic ramp. Setting DB28 to 0 disables the parabolic ramp.

Interrupt

DB[27:26] determine which type of interrupt is used. This feature is used for reading back the INT and FARC value of a ramp at a given moment in time (rising edge on the TX_{DATA} pin triggers the interrupt). From these bits, frequency can be obtained. After readback, the sweep might continue or stop at the readback frequency.

FSK Ramp Enable

Setting DB25 to 1 enables the FSK ramp. Setting DB25 to 0 disables the FSK ramp.

Ramp 2 Enable

Setting DB24 to 1 enables the second ramp. Setting DB24 to 0 disables the second ramp.

Deviation Select

Setting DB23 to 0 chooses the first deviation word. Setting DB23 to 1, chooses the second deviation word.

4-Bit Deviation Offset Word

DB[22:19] determine the deviation offset. The deviation offset affects the deviation resolution.

16-Bit Deviation Word

DB[18:3] determine the signed deviation word. The deviation word defines the deviation step.

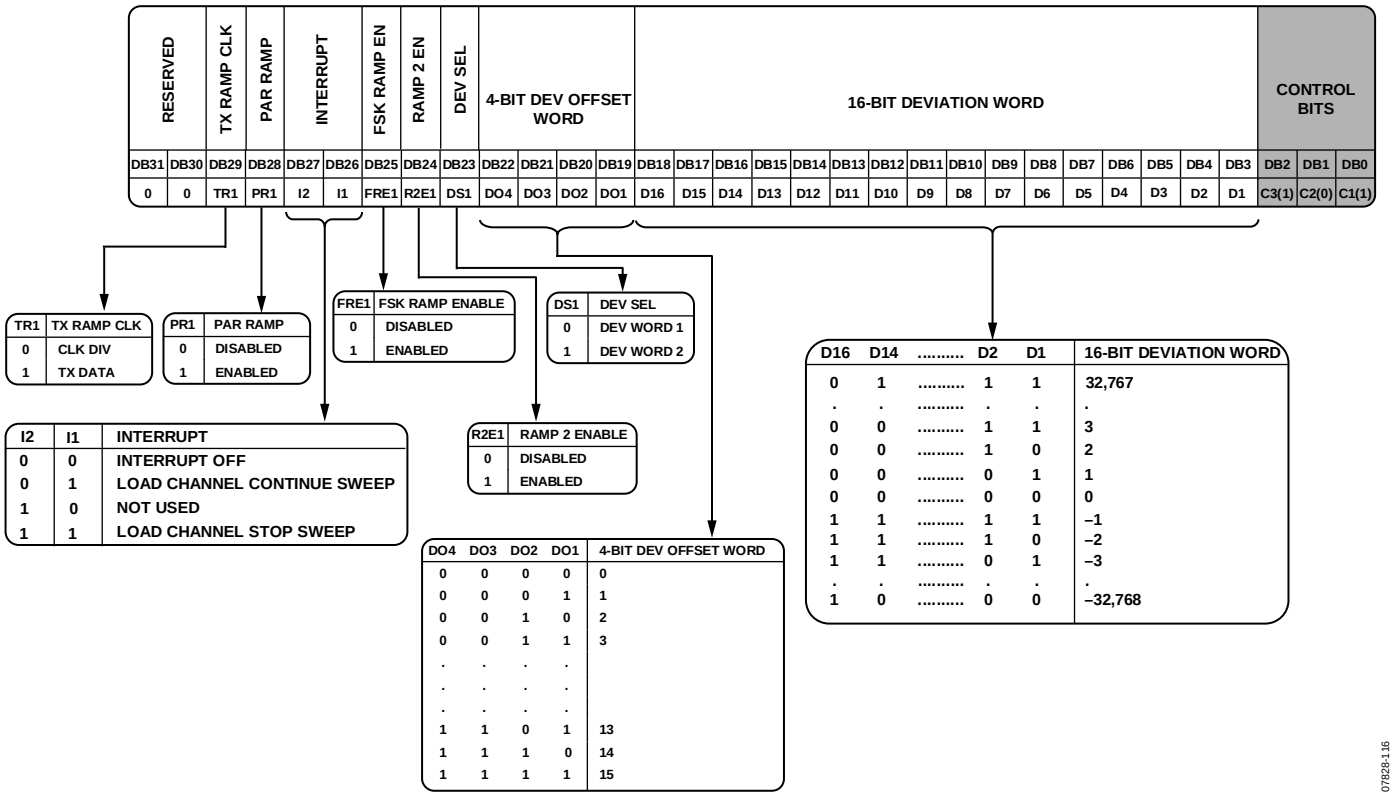


Figure 23. Deviation Register (R5) Map

STEP REGISTER (R6) MAP

With Register R6 DB[2:0] set to [1, 1, 0], the on-chip step register is programmed as shown in Figure 24.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Step SEL

Setting DB23 to 0 chooses Step Word 1. Setting DB23 to 1 chooses Step Word 2.

20-Bit Step Word

DB[22:3] determine the step word. Step word is a number of steps in the ramp.

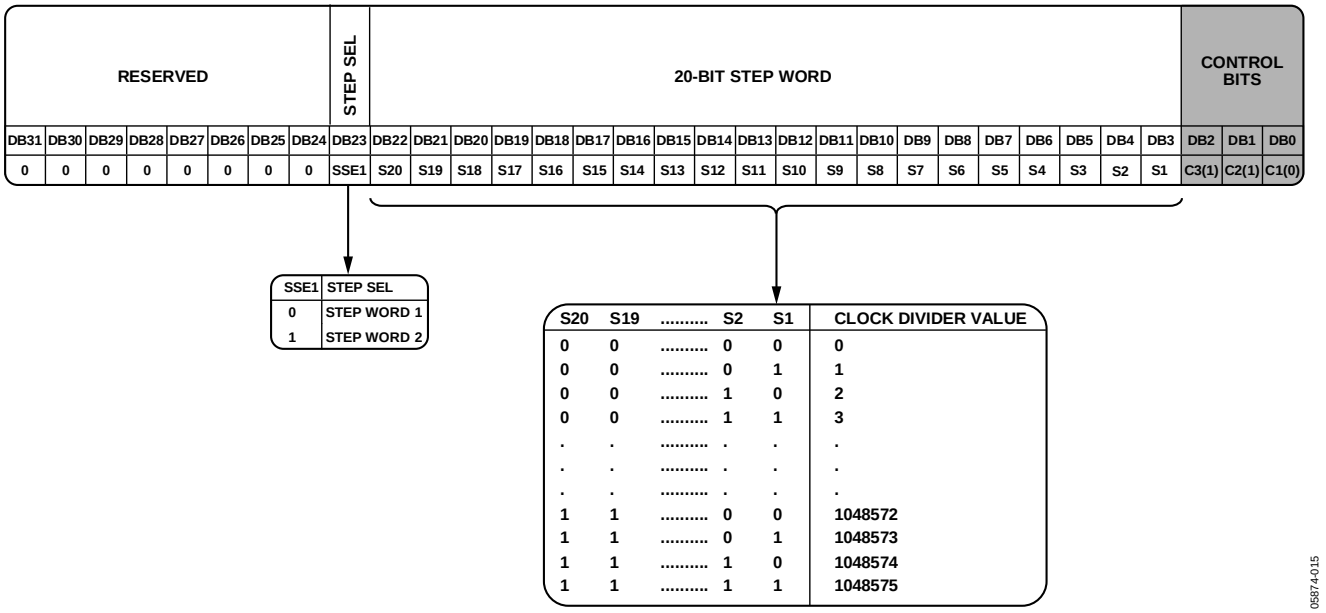


Figure 24. Step Register (R6) Map

DELAY REGISTER (R7) MAP

With Register R7 DB[2:0] set to [1, 1, 1], the on-chip delay register is programmed as shown in Figure 25.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Tri Del

Setting DB22 to 1 enables the delay between triangular ramps.

Setting DB22 to 0 enables the delay between clipped triangular ramps. This setting works only for triangular ramp and when Ramp Delay is activated. Please refer to the Delay Between Ramps section on Page 27 for more details.

Sing Full Tri

Setting DB21 to 1 enables the single full triangle function.

Setting DB21 to 0 disables this function. Please refer to the Waveform Generation section on Page 24 for more details.

TX RB

If DB20 is set to 1 logic high on TX_{DATA} activates the ramp.

Setting DB20 to 0 disables this function.

Fast Ramp

Setting DB19 to 1 activates the triangular waveform with two different slopes. It can be used as an alternative to sawtooth ramp as it mitigates the overshoot at the end of ramp in waveform. It is achieved by changing the top frequency to the bottom frequency in a series of small steps instead of one big step. Setting DB19 to 0 disables this function. Please see the Ramp complete signal to Muxout section on Page 29.

Ramp Delay Fast Lock

Setting DB18 to 1 enables the ramp delay fast-lock function. Setting DB18 to 0 disables this function.

Ramp Delay

Setting DB17 to 1 enables the ramp delay function. Setting DB17 to 0 disables this function.

Delay Clock Select

Setting DB16 to 0 selects the PFD clock as the delay clock. Setting DB16 to 1 selects PFD × MOD_DIV (MOD_DIV set by DB[14:3] in Register R2) as delay clock.

Delayed Start Enable

Setting DB15 to 1 enables delayed start. Setting DB15 to 0 disables delayed start.

12-Bit Delayed Start Word

DB[14:3] determine the delay start word. The delay start word affects the duration of the ramp start delay.

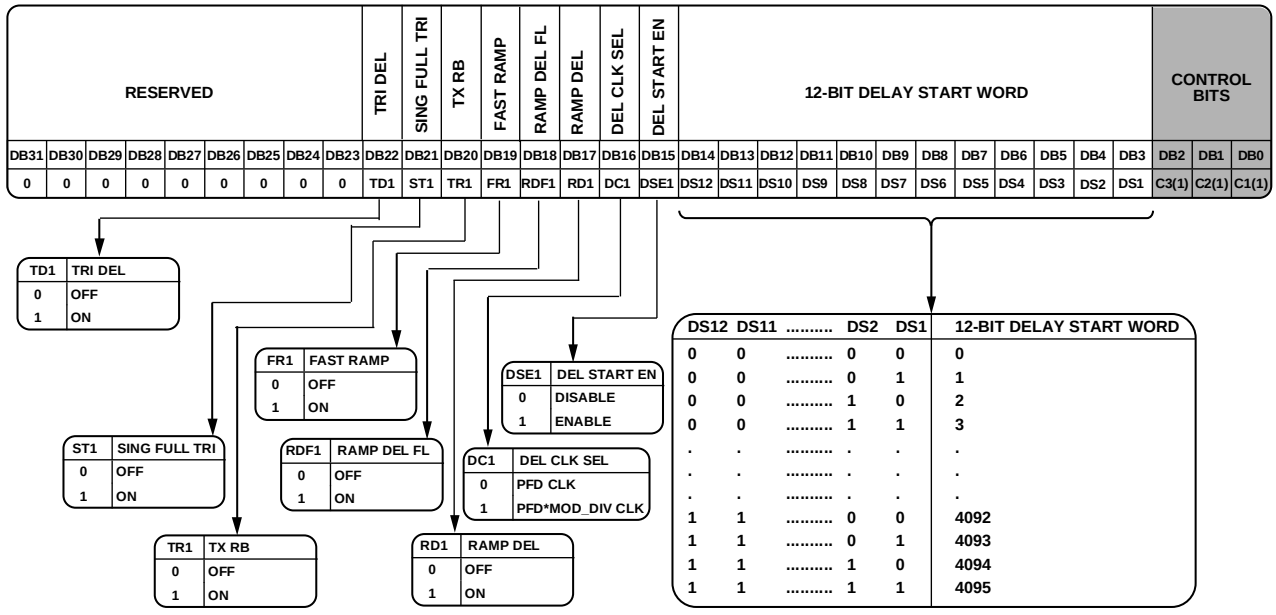


Figure 25. Delay Register (R7) Map

APPLICATIONS INFORMATION

INITIALIZATION SEQUENCE

After powering up the part, administer the following programming sequence:

1. Delay register (R7)
2. Step register (R6)—load the step register (R6) twice, first with STEP SEL = 0 and then with STEP SEL = 1
3. Deviation register (R5)—load the deviation register (R5) twice, first with DEV SEL = 0 and then with DEV SEL = 1
4. Test register (R4)
5. Function register (R3)
6. R-divider register (R2)
7. LSB FRAC register (R1)
8. FRAC/INT register (R0)

RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer should be programmed:

$$RF_{OUT} = [N + (FRAC/2^{25})] \times [f_{PFD}] \quad (4)$$

where:
RF_{OUT} is the RF frequency output.
N is the integer division factor.
$FRAC$ is the fractionality.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (5)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit (0 or 1).
R is the RF reference division factor.
T is the reference divide-by-2 bit (0 or 1).

For example, in a system where a 12.102 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available, the frequency resolution is

$$f_{RES} = REF_{IN}/2^{25} \quad (6)$$

$$f_{RES} = 100\ MHz/2^{25}$$

$$= 2.98\ Hz$$

From Equation 5,

$$f_{PFD} = [100\ MHz \times (1 + 0)/1] = 100\ MHz$$
$$12.102\ GHz = 100\ MHz \times (N + FRAC/2^{25})$$

Calculating N and FRAC values,

$$N = int(RF_{OUT}/f_{PFD}) = 121$$
$$FRAC = F_{MSB} \times 2^{13} + F_{LSB}$$
$$F_{MSB} = int(((RF_{OUT}/f_{PFD}) - N) \times 2^{12}) = 81$$
$$F_{LSB} = int(((((RF_{OUT}/f_{PFD}) - N) \times 2^{12}) - F_{MSB}) \times 2^{13}) = 671088$$

where:
F_{MSB} is the 12-bit MSB FRAC value in Register R0.
F_{LSB} is the 13-bit LSB FRAC value in Register R1.
int() makes an integer of the argument in parentheses.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB.

It is important to note that the PFD cannot be operated above 110 MHz due to a limitation in the speed of the Σ-Δ circuit of the N-divider.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

In fast-locking applications, a wide loop filter bandwidth is required for fast frequency acquisition, resulting in increased integrated phase noise and reduced spur attenuation. Using cycle slip reduction, the loop bandwidth can be kept narrow to reduce integrated phase noise and attenuate spurs while still realizing fast lock times.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared with the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction, slowing down the lock time dramatically. The ADF4159 contains a cycle slip reduction circuit to extend the linear range of the PFD, allowing faster lock times without loop filter changes.

When the ADF4159 detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Stability is maintained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4159 turns on another charge pump cell. This continues until the ADF4159 detects that the VCO frequency has gone past the desired frequency. It then begins to turn off the extra charge pump cells one by one until they are all turned off and the frequency is settled.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB28 in the R-divider register (Register R2) to 1 enables cycle slip reduction. Note that a 45% to 55% duty cycle is needed on the signal at the PFD in order for CSR to operate correctly. The reference divide-by-2 flip-flop can help to provide a 50% duty cycle at the PFD. For example, if a 100 MHz reference frequency is available and the user wants to run the PFD at 10 MHz, setting the R-divide factor to 10 results in a 10 MHz PFD signal that is not 50% duty cycle. By setting the R-divide factor to 5 and enabling the reference divide-by-2 bit, a 50% duty cycle 10 MHz signal can be achieved.

Note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is negative.

MODULATION

The ADF4159 can operate in frequency shift keying (FSK) or phase shift keying (PSK) mode.

Frequency Shift Keying (FSK)

FSK is implemented by setting the ADF4159 N-divider up for the center frequency and then toggling the TX_{DATA} pin. The deviation from the center frequency is set by

$$f_{DEV} = (f_{PFD}/2^{25}) \times (DEV \times 2^{DEV\_OFFSET}) \quad (7)$$

where:
DEV is a 16-bit word.
DEV_OFFSET is a 4-bit word.
f_{PFD} is the PFD frequency.

The ADF4159 implements this by incrementing or decrementing the set N-divide value by DEV × 2^{DEV_OFFSET}.

Phase Shift Keying (PSK)

When the ADF4159 is set up in PSK mode, it is possible to toggle the output phase of the ADF4159 between 0° and 180°. The TX_{DATA} pin controls the phase.

FSK Settings Worked Example

For example, take an FSK system operating at 5.8 GHz, with a 25 MHz PFD, 250 kHz deviation and DEV_OFFSET = 4. Rearrange Equation 4 as follows

$$DEV = \frac{f_{DEV}}{\frac{f_{PFD}}{2^{25}} \times 2^{DEV\_OFFSET}} \quad (8)$$

$$DEV = \frac{250\ \text{kHz}}{\frac{25\ \text{MHz}}{2^{25}} \times 2^{4}} = 20{,}971.52$$

The DEV value is rounded to 20,972. Toggling the TX_{DATA} pin causes the frequency to hop between ±250 kHz frequencies from the programmed center frequency.

WAVEFORM GENERATION

The ADF4159 is capable of generating four types of waveforms in the frequency domain: single ramp burst, single triangular burst, single sawtooth burst, continuous sawtooth ramp, and continuous triangular ramp. Figure 26 through Figure 30 show the types of waveforms available.

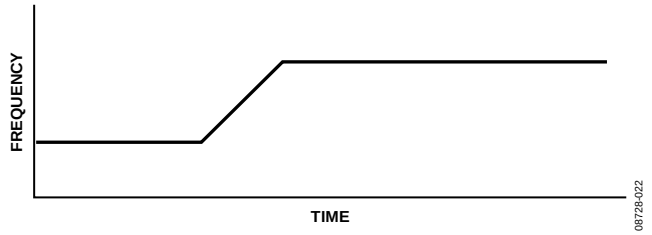


Figure 26. Single Ramp Burst

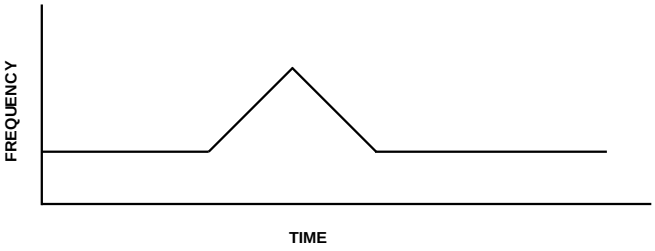


Figure 27 Single Triangle Burst

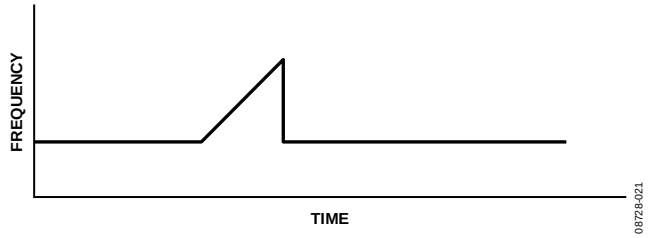


Figure 28. Single Sawtooth Burst

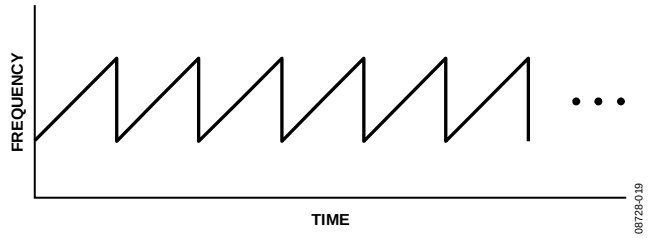


Figure 29. Continuous Sawtooth Ramp

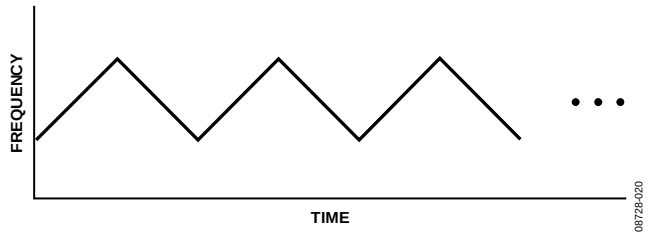


Figure 30. Continuous Triangular Ramp

Waveform Deviations and Timing

Figure 31 shows a version of a burst or ramp. The key parameters that define a burst or ramp are

- Frequency deviation
- Timeout interval
- Number of steps

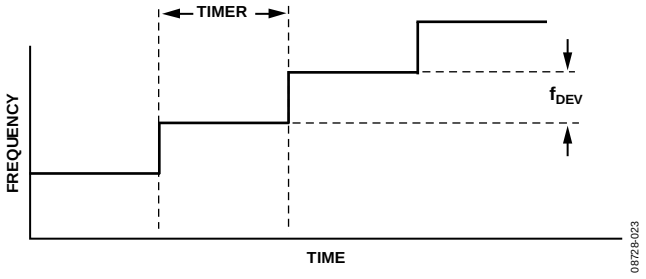


Figure 31. Waveform Timing

Frequency Deviation

The frequency deviation for each frequency hop is set by

$$f_{DEV} = (f_{PFD}/2^{25}) \times (DEV \times 2^{DEV\_OFFSET}) \quad (9)$$

where:
DEV is a 16-bit word.
DEV_OFFSET is a 4-bit word.

Timeout Interval

The time between each frequency hop is set by

$$Timer = CLK_1 \times CLK_2 \times (1/f_{PFD}) \quad (10)$$

where:
CLK_1 and CLK_2 are 12-bit clock values (12-bit MOD divider in R2, 12-bit clock divider in R4—CLK DIV set as RAMP DIV).
f_{PFD} is the PFD frequency.

Number of Steps

A 20-bit step value defines the number of frequency hops that take place. The INT value cannot be incremented by more than $2^8 = 256$ from its starting value.

Single Ramp Burst

The most basic waveform is the single ramp burst. All other waveforms are slight variations on this.

In the single ramp burst, the ADF4159 is locked to the frequency defined in the FRAC/INT register. When the ramp mode is enabled, the ADF4159 increments the N-divide value by DEV × 2^{DEV_OFSET}, causing a frequency shift, f_{DEV}, on each timer interval. This happens until the set number of steps has taken place. The ADF4159 then retains the final N-divide value.

Single Triangular Burst

The triangular burst is similar to the single ramp burst. However, when the steps have been completed, the ADF4159 begins to decrement the N-divide value by *DEV* × 2DEV_OFFSET on each timeout interval.

Single Sawtooth Burst

In the single sawtooth burst, the N-divide value is reset to its initial value on the next timeout interval after the number of steps has taken place. The ADF4159 retains this N-divide value.

Sawtooth Ramp

The sawtooth ramp is a repeated version of the single sawtooth burst. The waveform repeats until the ramp is disabled.

Triangular Ramp

The triangular ramp is similar to the single ramp burst. However, when the steps have been completed, the ADF4159 begins to decrement the N-divide value by DEV × 2^{DEV_OFFSET} on each timeout interval. When the number of steps has again been completed, it reverts to incrementing the N-divide value. Repeating this creates a triangular waveform. The waveform repeats until the ramp is disabled.

FMCW Radar Ramp Settings Worked Example

Take as an example, an FMCW radar system requiring the RF LO to sawtooth ramp over a 50 MHz range every 2 ms. The PFD frequency is 25 MHz, and the RF output range is 5800 MHz to 5850 MHz.

The frequency deviation for each hop in the ramp is set to ~250 kHz.

The frequency resolution of ADF4159 is calculated as follows:

$$f_{RES} = f_{PFD}/2^{25} \quad (11)$$

Numerically:

$$f_{RES} = 25\ MHz/2^{25} = 0.745\ Hz$$

The DEV_OFFSET is calculated after rearranging Equation 9:

$$DEV\_OFFSET = \log_2(f_{DEV}/(f_{RES} \times DEV_{MAX})) \quad (12)$$

Expressed in $\log_{10}(x)$, Equation 10 can be transformed into the following equation:

$$DEV\_OFFSET = \log_{10}(f_{DEV}/(f_{RES} \times DEV_{MAX}))/\log_{10}(2) \quad (13)$$

where:
$DEV_{MAX} = 2^{15}$ – *Maximum of the Deviation Word*.
f_{DEV} = frequency deviation.
DEV_OFFSET = a 4-bit word.

Using Equation 13, DEV_OFFSET is calculated as follows

$$DEV\_OFFSET = \log_{10}(250\ kHz/(0.745\ Hz \times 2^{15}))/\log_{10}(2) = 3.356$$

After rounding, DEV_OFFSET = 4.

From DEV_OFFSET, the resolution of frequency deviation can be calculated as follows

$$f_{DEV\_RES} = f_{RES} \times 2^{DEV\_OFFSET} \quad (14)$$

$$f_{DEV\_RES} = 0.745\ Hz \times 2^4 = 11.92\ Hz$$

To calculate the DEV word, use Equation 12.

$$DEV = f_{DEV}/(f_{RES} \times 2^{DEV\_OFFSET}) \quad (15)$$

$$DEV = \frac{250\ kHz}{\frac{25\ MHz}{2^{25}} \times 2^4} = 20{,}971.52$$

Rounding this to 20,972 and recalculating using Equation 9 to get the actual deviation frequency, f_{DEV}, thus produces the following:

$$f_{DEV} = (25\ MHz/2^{25}) \times (20{,}972 \times 2^4) = 250.006\ kHz$$

The number of f_{DEV} steps required to cover the 50 MHz range is 50 MHz/250.006 kHz = 200. To cover the 50 MHz range in 2 ms, the ADF4159 must hop every 2 ms/200 = 10 μs.

Rearrange Equation 10 to set the timer value (and fix CLK_2 to 1):

$$CLK_1 = Timer \times f_{PFD}/CLK_2 = 10\ \mu s \times 25\ MHz\ /1 = 250$$

To summarize the settings: DEV = 20,972, number of steps = 200, CLK_1 = 250, CLK_2 = 1 (R4—CLK DIV set as RAMP DIV). Using these settings, program the ADF4159 to a center frequency of 5800 MHz, and enable the sawtooth ramp to produce the required waveform. If a triangular ramp was used with the same settings, the ADF4159 would sweep from 5800 MHz to 5850 MHz and back down again. The entire sweep would take 4 ms.

Activating the Ramp

After setting all of the previous parameters, the ramp must be activated. It is achieved by choosing the desired type of ramp (DB[11:10] in Register R3) and starting the ramp (DB31 = 1 in Register R0).

Ramp programming sequence

The setting of parameters described in the FMCW Radar Ramp Settings Worked Example section on Page 25 and the activation of the ramp described in the Activating the Ramp section on Page 26 should be done by the following register write order.

1. Delay register (R7)
2. Step register (R6)
3. Deviation register (R5)
4. Test register (R4)
5. Function register (R3)
6. R-divider register (R2)
7. LSB FRAC register (R1)
8. FRAC/INT register (R0)

OTHER WAVEFORMS

Two Ramp Rates

This feature allows for two ramps with different step and deviation settings. It also allows the ramp rate to be reprogrammed while another ramp is running.

Example

For example, if

- PLL is locked to 5790 MHz and f_{PFD} = 25MHz .
- Ramp 1 jumps 100 steps, each of which lasts 10 μs and has a frequency deviation of 100 kHz.
- Ramp 2 jumps 80 steps, each of which lasts 10 μs and has a frequency deviation of 125 kHz.

Then,

1. DB24 in Register R5 should be set to 1, which activates Ramp 2 rates mode.
2. Program Ramp 1 and Ramp 2 as follows to get two ramp rates:
   Ramp 1: Register R5 DB[18:3] = 16,777, DB[22:19] = 3 with DB23 = 0; Register R6 DB[22:3] = 100, DB23 = 0.
   Ramp 2: Register R5 DB[18:3] = 20,972, DB[22:19] = 3 with DB23 = 1; Register R6 DB[22:3] = 80, DB23 = 1.

The resulting ramp with two various rates is shown in Figure 32. Eventually, the ramp must be activated as described in Activating the Ramp section on Page 26.

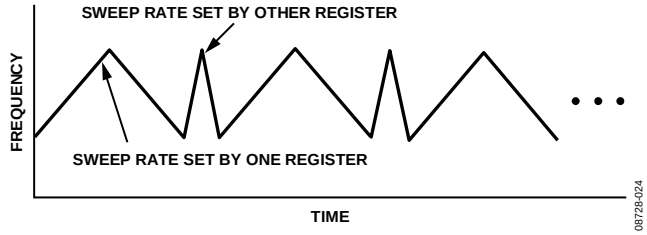


Figure 32. Dual Sweep Rate

Ramp Mode with FSK Signal on Ramp

In traditional approaches a FMCW radars used either linear frequency modulation (LFM) or FSK modulation. These modulations used separately introduce ambiguity between measured distance and velocity, especially in multitarget situations. To overcome this issue and enable unambiguous (range – velocity) multitarget detection, use a ramp with FSK on it.

Example

For example, if

- PLL is locked to 5790 MHz and f_{PFD} = 25MHz.
- There are 100 steps each of which lasts 10 μs and has a deviation of 100 kHz.
- The FSK signal is 25 kHz.

Then,

1. Program the ramp as described in the FMCW Radar Ramp Settings Worked Example section on Page 25. While doing that DB23 in Register R5 and DB23 in Register R6 should be set to 0.
2. Set the bits in Register R5 as follows to program FSK on ramp to 25 kHz:
   DB[18:3] = 4194 (deviation word), DB[22:19] = 3 (deviation offset), DB23 = 1 (deviation select for FSK on ramp), and DB25 = 1 (ramp with FSK enabled).

An example of ramp with FSK on the top of it is shown in Figure 33. Eventually, the ramp must be activated as described in Activating the Ramp section on Page 26.

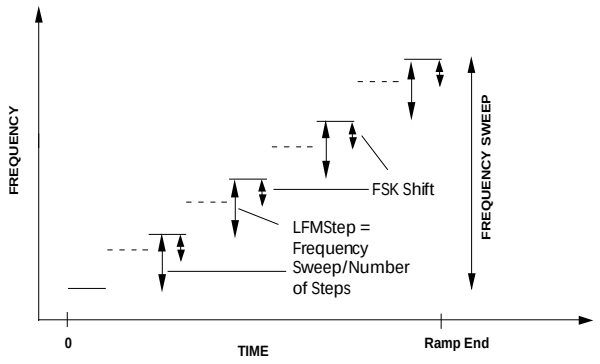


Figure 33. Combined FSK and LFM Waveform (N Corresponds to the Number of LFM Steps)

Delayed Start

A delayed start can be used with two different parts to control the start time. The idea of delayed start is shown in Figure 34.

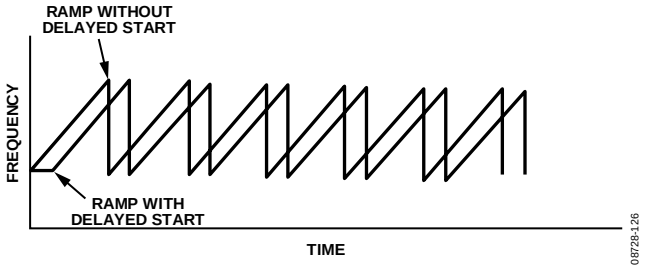


Figure 34. Delayed Start of Sawtooth Ramp

Example

For example, to program a delayed start with two different parts to control the start time,

1. Set DB15 in Register R7 to 1 to enable the delayed start of ramp option.
2. Set Bit DB16 in Register R7 to 0 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp on the first part is delayed by 5 μs. f_{PFD} = 25MHz . The delay is calculated as follows:

   $Delay = t_{PFD} \times Delay\ Start\ Word$
   $= 40\ ns \times 125 = 5\ \mu s$

3. Set Bit DB16 in Register R7 to 1 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp on the second part is delayed by 125 μs. Use the following formula for calculating the delay:

   $Delay = t_{PFD} \times MOD \times Delay\ Start\ Word$
   $= 40\ ns \times 25 \times 125 = 125\ \mu s$

Eventually, the ramp must be activated as described in Activating the Ramp section on Page 26.

Delay Between Ramps

This feature adds a delay between bursts in ramp. Figure 35, Figure 36 and Figure 37 show a delay between ramps in sawtooth, triangular and clipped triangular mode respectively.

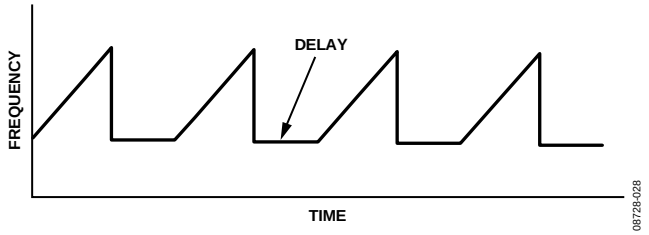


Figure 35. Delay Between Ramps for Sawtooth Mode

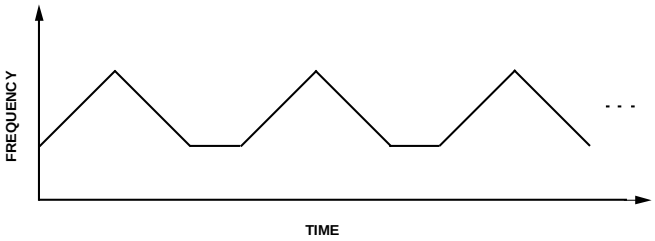


Figure 36 Delay between ramps for triangular mode

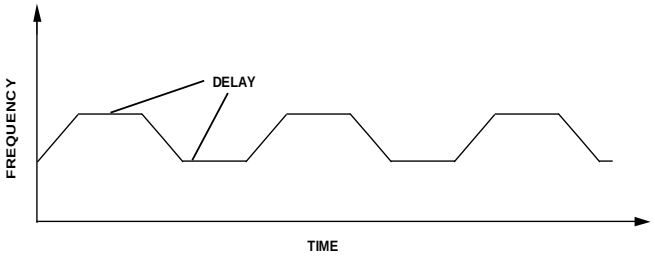


Figure 37 Delay between ramps for clipped triangular mode

Example

For example, to add a delay between bursts in a ramp,

1. Set DB17 in Register R7 to 1 to enable delay between ramps option.
2. Set Bit DB16 in Register R7 to 0 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp by 5 μs. f_{PFD} = 25MHz. The delay is calculated as follows:

   $Delay = t_{PFD} \times Delay\ Start\ Word$
   $= 40\ ns \times 125 = 5\ \mu s$

   If a longer delay is needed, for example, 125 μs, Bit DB16 in Register R7 should be set to 1 and the 12-bit delay start word (DB[14:3] in Register R7) should be set to 125. The delay is calculated as follows

   $Delay = t_{PFD} \times MOD \times Delay\ Start\ Word$
   $= 40\ ns \times 25 \times 125 = 125\ \mu s$

There is also a possibility to activate fast-lock operation for the first period of delay. This is done by setting Bit DB18 in

Register R7 to 1. This feature is useful for sawtooth ramps to mitigate the frequency overshoot on the transition from one sawtooth to the next. Eventually, the ramp must be activated as described in Activating the Ramp section on Page 25.

Two Ramp Rates Mode with Delay

This mode combines the Two Ramp Rates with Delay Between Ramps.

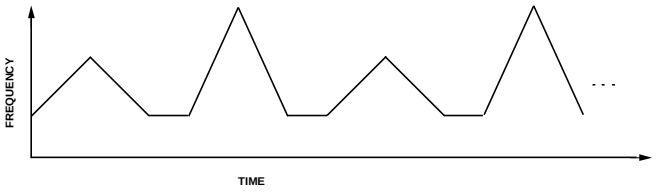


Figure 38 Two Ramp Rates Mode with Delay

First the Two Ramp Rates should be programmed as described in the Example in Two Ramp Rates Section on Page 26 and then the delay should be programmed as described in Delay Between Ramps Section on Page 27.

Nonlinear Ramp Mode

The ADF4159 is capable of generating a parabolic ramp. The output frequency is generated according to the following equation:

$$f_{OUT}(n + 1) = f_{OUT}(n) + n \times f_{DEV} \quad (16)$$

where:
f_{OUT} is output frequency.
f_{DEV} is frequency deviation.
n is step number.

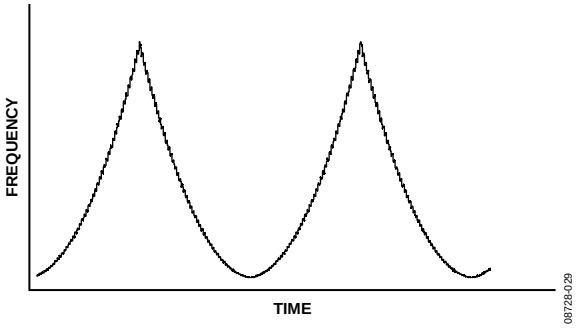


Figure 39. Parabolic Ramp

The following example explains how to set up and use this function.

Example

f_{OUT} = 5790 MHz

f_{DEV} = 100 kHz

Number of steps = 50

Duration of a single step = 10 μs

Ramp mode must be either continuous triangular (Register R3, DB[11:10] = 01) or single ramp burst (Register R3, DB[11:10] = 11) or single triangular burst (Register R3, DB[11:10] = 11 and Register R7, DB21 = 1).

In the first case, the generated frequency range is calculated as follows:

$$\Delta f = f_{DEV} \times (Number\ of\ Steps + 2) \times (Number\ of\ Steps + 1)/2$$

$$= 132.6\ MHz$$

In the second case, the generated frequency range is calculated as follows:

$$\Delta f = f_{DEV} \times (Number\ of\ Steps + 1) \times Number\ of\ Steps/2$$

$$= 127.5\ MHz$$

The timer is set in the same way as for its linear ramps described in the Waveform Generation section on Page 24.

Activation of the parabolic ramp is achieved by setting Bit DB28 in Register R5 to 1.

Next the counter reset (DB3 in Register R3) should be set first to 1 and then to 0.

Eventually, the ramp must be activated as described in the Activating the Ramp section on Page 25.

Fast Ramp Mode

The ADF4159 is capable of generating a Fast Ramp.

The Fast Ramp is a triangular ramp with two different slopes. Figure 40 shows the Fast Ramp.

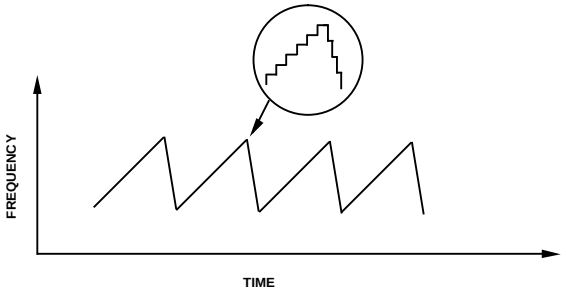


Figure 40 Fast Ramp Mode

In order to activate this waveform triangular type of waveform should be chosen. DB19 in register 7 should be set to 1. For programming the up ramp CLK DIV SEL should be set to LOAD CLK DIVIDER 1, DEV SEL should be set to DEV WORD 1 and STEP SEL should be set to STEP WORD 1. Then Timer, DEV, DEV OFFSET and STEP WORD should be calculated and programmed as described in FMCW Radar Ramp Settings Worked Example. For programming the down ramp CLK DIV SEL should be set to LOAD CLK DIVIDER 2, DEV SEL should be set to DEV WORD 2 and STEP SEL should be set to STEP WORD 2. Then Timer, DEV, DEV OFFSET and STEP WORD should be calculated and programmed again.

Ramp complete signal to Muxout

Ramp complete signal on Muxout is shown in Figure 41.

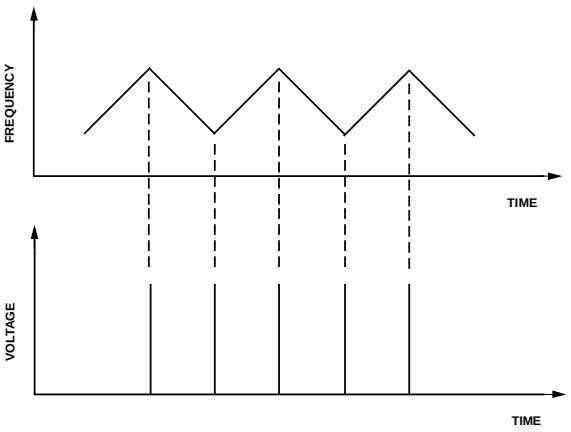


Figure 41 Ramp Complete Signal on Muxout

In order to activate this function DB[30:27] = 1111 in Register 0 and DB[25:21] = 00011 in Register 4

Interrupt Modes and Frequency Readback

Interrupt modes are triggered from the rising edge of TX_{DATA}. Depending on the settings of DB[27:26] in Register R5, the modes in Table 7 are activated.

Table 7. Interrupt Modes

Mode	Action
DB[27:26] = 00	Interrupt is off
DB[27:26] = 01	Interrupt on TX_{DATA}, sweep continues
DB[27:26] = 11	Interrupt on TX_{DATA}, sweep stops

When an interrupt takes place, the data consisting of the INT and FRAC values can be read back via MUXOUT. The data is made up of 37 bits, 12 of which represent the INT value and 25 the FRAC value.

The idea of frequency readback is shown in Figure 42.

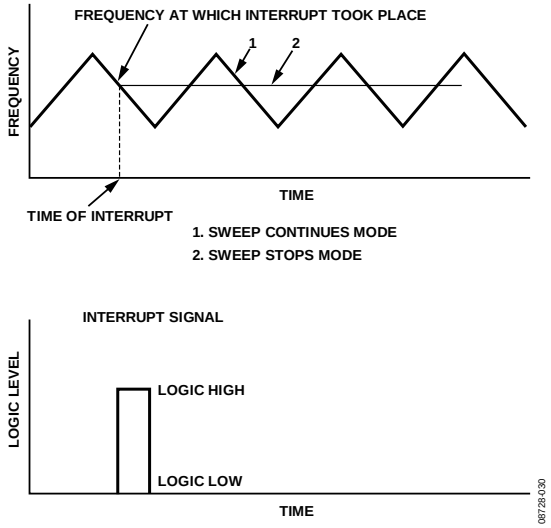


Figure 42. Interrupt and Frequency Readback

Note that DB[22:21] in Register R4 should be set to 2 and DB[30:27] in Register R0 (MUXOUT control) should be set to 15 (1111).

The mechanism of how single bits are read back is shown in Figure 43.

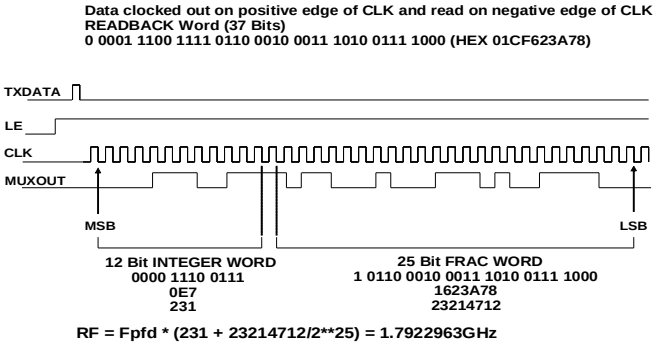


Figure 43 Reading Back Single Bits to Determine the Output Frequency at the Moment of Interrupt

For continuous frequency readback the following sequence should be used:

- Register 0 write
- LE high
- Pulse on TX_{DATA}

Frequency readback (as described at the beginning of the

- Interrupt Modes and Frequency Readback section on Page 29 and Figure 43)
- Pulse on TX_{DATA}
- Register R4 write

Frequency readback (as described at the beginning of the

- Interrupt Modes and Frequency Readback section on Page 29 and Figure 43)
- Pulse on TX_{DATA}

The sequence is also shown in Figure 44.

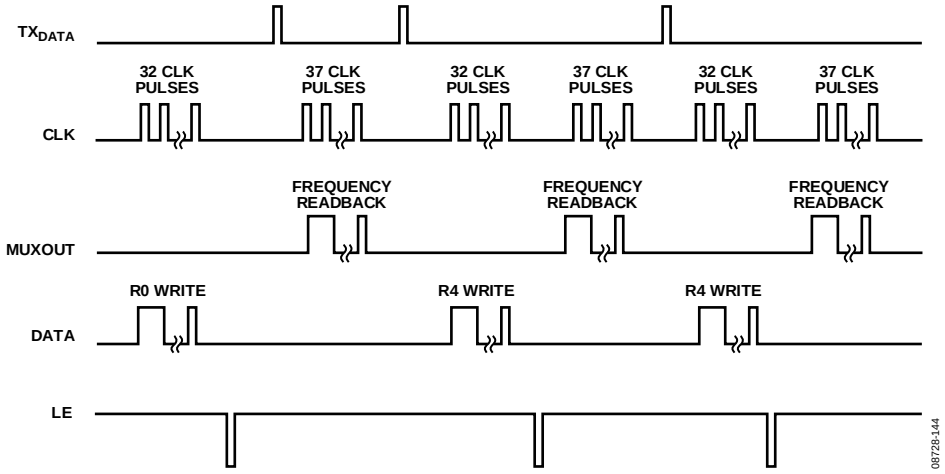


Figure 44. Continuous Frequency Readback

FAST LOCK MODE

ADF4159 can operate in fast lock mode. In this mode charge pump current is boosted and additional resistors are connected to maintain the stability of the loop.

Fast-Lock Timer and Register Sequences

If the fast-lock mode is used, a timer value needs to be loaded into the PLL to determine the time spent in wide bandwidth mode.

When the DB[20:19] bits in Register 4 (R4) are set to 01 (fast-lock divider), the timer value is loaded via the 12-bit clock divider value. To use fast lock, the PLL must be written to in the following sequence:

1. Initialization sequence (see the Initialization Sequence section on Page 23). This should only be performed once after powering up the part.
2. Load Register R4 DB[16:15] = 01 and the chosen fast-lock timer value (DB[18:7]).
3. Load Register R2 with the chosen MOD divider value (DB[14:3]) if longer time in wide loop bandwidth is required.

Note that the duration that the PLL remains in wide bandwidth is equal to the MOD × fast-lock timer/f_{PFD}, where MOD is the 12-bit MOD divider in Register R2.

In addition, note that the fast-lock feature doesn't work in ramp mode.

Fast Lock: An Example

If a PLL has a reference frequency of 13 MHz, that is, f_{PFD} = 13 MHz, as well as MOD = 10 (12-bit MOD divider in Register R2) and a required lock time of 50 μs, the PLL is set to wide bandwidth for 40 μs.

If the time period set for the wide bandwidth is 40 μs, then

Fast-Lock Timer Value = Time in Wide Bandwidth × f_{PFD}/MOD

Fast-Lock Timer Value = 40 μs × 13 MHz /10 = 52.

Therefore, 52 must be loaded into the clock divider value in Register R4 in Step 1 of the sequence described in the Fast-Lock Timer and Register Sequences section on Page 30.

Fast Lock: Loop Filter Topology

To use fast-lock mode, an extra connection from the PLL to the loop filter is needed. The damping resistor in the loop filter must be reduced to ¼ of its value while in wide bandwidth mode. This is required because the charge pump current is increased by 16 while in wide bandwidth mode, and stability must be ensured. To further enhance stability and mitigate frequency overshoot while frequency change (in wide bandwidth mode), Resistor R3 is connected. During fast lock, the SW1 pin is shorted to ground and SW2 is connected to CP (it is done by setting Bits DB[20:19] in Register R4 to 01—fast lock divider). The following two topologies can be used:

- Divide the damping resistor (R1) into two values (R1 and R1A) that have a ratio of 1:3 (see Figure 45).
- Connect an extra resistor (R1A) directly from SW1, as shown in Figure 46. The extra resistor must be chosen such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to ¼ of the original value of R1.

For both of the topologies, the ratio R3:R2 should equal 1:4.

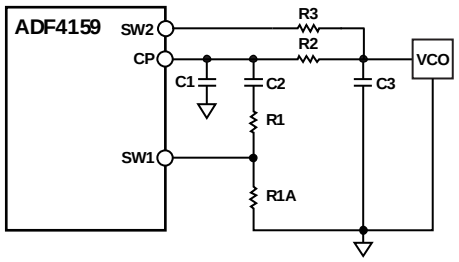


Figure 45 Fast-Lock Loop Filter Topology—Topology 1

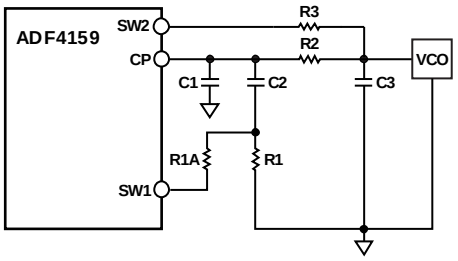


Figure 46. Fast-Lock Loop Filter Topology—Topology 2Spur Mechanisms

The fractional interpolator in the ADF4159 is a third-order Σ-Δ modulator (SDM) with a 25-bit fixed modulus (MOD). The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD. The various spur mechanisms possible with fractional-N synthesizers and how they affect the ADF4159 are discussed in this section.

SPUR MECHANISMS

The fractional interpolator in the ADF4159 is a third-order Σ-Δ modulator (SDM) with a 25-bit fixed modulus (MOD). The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD. The various spur mechanisms possible with fractional-N synthesizers and how they affect the ADF4159 are discussed in this section.

Fractional Spurs

In most fractional synthesizers, fractional spurs can appear at the set channel spacing of the synthesizer. In the ADF4159, these spurs do not appear. The high value of the fixed modulus in the ADF4159 makes the SDM quantization error spectrum look like broadband noise, effectively spreading the fractional spurs into noise.

Integer Boundary Spurs

Interactions between the RF VCO frequency and the PFD frequency can lead to spurs known as integer boundary spurs. When these frequencies are not integer related (which is the purpose of the fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the PFD and the VCO frequency.

These spurs are named integer boundary spurs because they are more noticeable on channels close to integer multiples of the PFD where the difference frequency can be inside the loop bandwidth. These spurs are attenuated by the loop filter on channels far from integer multiples of the PFD.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is the feedthrough of low levels of on-chip reference switching noise out through the RF_{IN} pins back to the VCO, resulting in reference spur levels as high as −90 dBc. Take care in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

Low Frequency Applications

The specification on the RF input is 0.5 GHz minimum; however, RF frequencies lower than this can be used if the minimum slew rate specification of 400 V/μs is met. An appropriate driver can be used to square up the RF signal before it is fed back to the ADF4159 RF input. The ADCMP553 is one such drivers.

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user implement PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL™ software. This software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

PCB DESIGN GUIDELINES FOR THE CHIP SCALE PACKAGE

The lands on the chip scale package (CP-24) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via. Connect the PCB thermal pad to AGND.

APPLICATION OF ADF4159 IN FMCW RADAR

The application of ADF4159 in FMCW radar is shown in Figure 47.

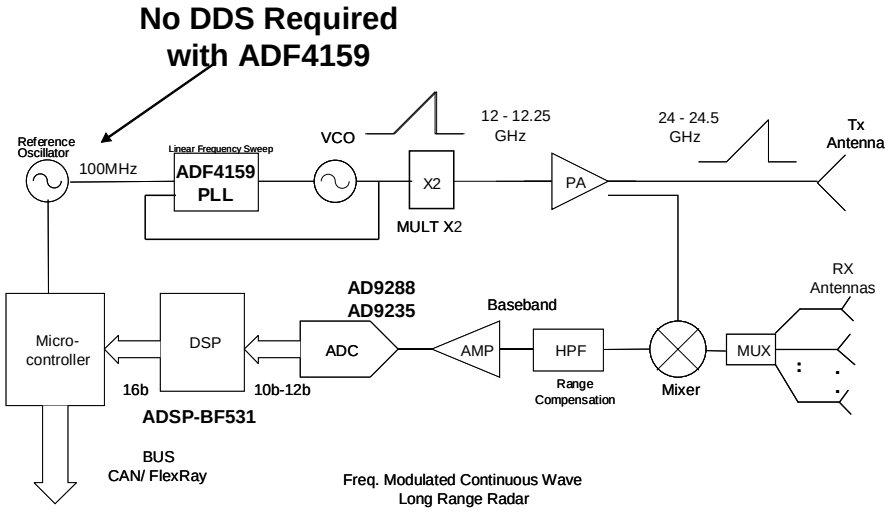
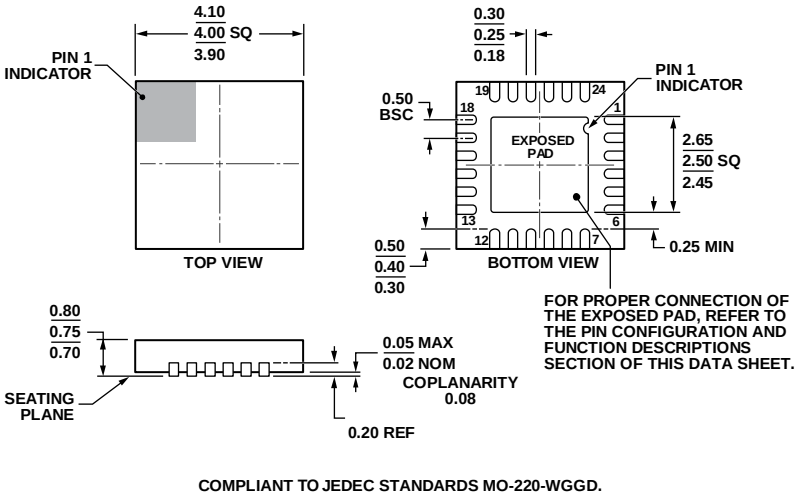


Figure 47. FMCW Radar with ADF4159

The ADF4159 in FMCW radar is used for generating ramps (sawtooth or triangle) that are necessary for this type of radar to operate. Traditionally, the PLL was driven directly by a direct digital synthesizer (DDS) to generate the required type of waveform. Due to the implemented waveform generating mechanism on the ADF4159, a DDS is no longer needed, which reduces cost. In addition, the PLL solution has advantages over another method (the DAC driving the VCO directly) for generating FMCW ramps, which suffered from VCO tuning characteristics nonlinearities requiring compensation. The PLL method gives highly linear ramps without the need for calibration.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 48. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-7)
Dimensions shown in millimeters

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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